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HARRITY & SNYDER, LLP 11240 WAPLES MILL ROAD SUITE 300 FAIRFAX, VA 22030			BATES, KEVIN T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Amendment

This Office Action is in response to a communication made on August 15, 2005.

Claims 1-5, 10, and 16-18 have been amended.

Claim 6 has been cancelled.

Claims 21-23 have been newly added.

Claims 1-5, 7, 9-13, 15-19, and 21-23 are pending in this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-11, 13, and 15 rejected under 35 U.S.C. 102(b) as being anticipated by Humphrey (4933846).

Regarding claim 10, Humphrey teaches in a network device that controls communication of data frames between stations (Column 6, lines 33 – 34), a method of storing data frame information (Column 4, lines 10 – 20), comprising:

receiving a plurality of data frames (Column 1, lines 42 – 48);

temporarily storing the received data frames in a plurality of receive devices

(Figure 5, element 354; Figure 6a, element 420 and 432), and

simultaneously transferring data frame information to at least a first memory and a second memory wherein the simultaneously transferring includes:

alternating the transferring data frame information from a first group of the receive devices to the first and second memories, and

alternating the transferring data frame information from a second group of the receive devices to the first and second memories, wherein when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62, where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented).

Regarding claim 11, Humphrey teaches the method of claim 10, further comprising: simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively (Column 5, lines 25 – 34).

Regarding claim 13, Humphrey teaches the method of claim 10, wherein the simultaneously transferring further includes:

sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus (Column 5, lines 5, lines 9 – 13; lines 25 – 34).

Regarding claim 15, Humphrey teaches the method of claim 10 further comprising: simultaneously retrieving data frame information from the first and second memories (Column 5, lines 19 – 21).

Regarding claim 22, Humphrey teaches the method of claim 10, wherein the alternating of the transferring of data frame information from the first group of receive devices to the first and second memories is performed each clock cycle (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62, where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented).

Claims 1-6, 9, 12, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey (4933846) in view of Mann (6021477).

Regarding claim 1, Humphrey teaches a network device configured to control communication of data frames between stations (Column 6, lines 33 – 34), comprising:

a plurality of receive devices corresponding to ports on the network device, the receive devices configured to receive data frames from the stations (Column 1, lines 42 – 48; Figure 1, element 114 and 116); and

an external memory interface configured to:

receive data from the plurality of receive devices,

transfer a portion of the data received from a first group of the receive devices to a first memory and a second memory in an alternating manner, and

transfer a portion of the data received from a second group of the received devices to the first memory and the second memory, in an alternating manner (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62, where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented, and wherein the first group of receive devices is the processor that is receiving information from host 1, and the second group of receive devices is the processor receiving information from host 2, Figure 1, element 114 and 116).

Humphrey does not explicitly indicate that the external interface is configured to generate odd address information when transferring data to the first memory and even address information when transferring data via the second memory

Mann teaches a memory interface with dual memories (Figure 2a, elements 24, 28, and 30). Mann teaches a system that generates odd address information when transferring data to the first memory and even address information when transferring data via the second memory (Column 2, lines 38 – 44, odd and even memories; Column 5, line 61 – Column 6, line 17, generating odd and even addresses).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claims 2, Humphrey teaches the network device of claim 1 wherein the external memory interface includes:

a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from one of the first group of receive devices and one of the second group of receive devices, respectively (Column 5, lines 25 – 34).

Regarding claims 3 and 12, Humphrey teaches the network device of claim 2 and 10, wherein the external memory interface is further configured to simultaneously transfer data one of the first group of receive devices to the first memory and of data

from one of the second group of receive devices to the second memory (Column 5, lines 5, lines 9 – 13).

Humphrey does not explicitly indicate that the data transfer is 8 bytes.

Mann discloses a memory interface with dual memories that discloses the transferred data can be 8 bytes wide (Column 1, lines 35 – 36; Column 2, lines 52 – 55 for the 8 bytes or 64 bits).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claim 4, Humphrey teaches the network device of claim 1, wherein the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second groups of receive devices to the first and second memories (Column 5, lines 5, lines 9 – 13; lines 25 – 34).

Regarding claim 5, Humphrey teaches the network device of claim 1, wherein the external memory interface is configured to simultaneously transfer data received from the first one of a first group of the receive devices via the first external memory bus and the second one of a second group of the receive devices via the second external memory bus (Column 5, lines 5 – 10).

Regarding claim 9, Humphrey teaches the network device of claim 1, the external memory interface is further configured to simultaneously retrieve data from the first and second memories (Column 5, lines 19 – 21).

Regarding claim 16, Humphrey teaches a data communication system for controlling the communication of data frames between stations (Column 6, lines 33 – 34), comprising:

- a plurality of receive devices configured to receive data frames from the stations (Column 1, lines 42 – 48; Figure 1, element 114 and 116);

- a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices (Column 5, lines 25 – 34);

- a switching device configured to:

- receive the data frame information, and

- simultaneously transfer data frame information from one of the first group of receive devices via a first external memory bus and data frame information from one of a second group of receive devices via a second external memory bus;

- a first memory configured to receive data frame information from the first external memory bus; and

- a second memory configured to receive data frame information from the second external memory bus, wherein the switching device is further configured to:

- transfer data frame information from the first group of receive devices to the first and second external memory buses in an alternating manner, and

- transfer data frame information from the second group of receive devices to the first and second external memory buses in an alternating manner (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62,

where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented).

Humphrey does not explicitly indicate that the external interface is configured to generate odd address information when transferring data to the first memory and even address information when transferring data via the second memory

Mann teaches a memory interface with dual memories (Figure 2a, elements 24, 28, and 30). Mann teaches a system that generates odd address information when transferring data to the first memory and even address information when transferring data via the second memory (Column 2, lines 38 – 44, odd and even memories; Column 5, line 61 – Column 6, line 17, generating odd and even addresses).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claim 17, Humphrey teaches the system of claim 16, further comprising: first and second multiplexers coupled to the first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured

to receive the selection signals from the scheduler and to output a portion of a data frame (Figure 6a, element 402, 416, and 428).

Regarding claim 18, Humphrey teaches the system of claim 17, wherein the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses (Column 5, lines 5, lines 9 – 13; lines 25 – 34; lines 39 – 54).

Regarding claim 19, Humphrey teaches the system of claim 16.

Humphrey does not explicitly indicate that the first memory is configured to store data words having odd addresses; and the second memory is configured to store data words having even addresses.

Mann teaches that the first memory is configured to store data words having odd addresses; and the second memory is configured to store data words having even addresses (Mann, Column 5, line 61 – Column 6, line 17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claim 21, Humphrey teaches the network device of claim 1, wherein the external memory interface is further configured to:

transfer data from one of the first group of receive devices to the first memory during a first clock cycle,

transfer data from one of the second group of receive devices to the second memory during the first clock,

transfer data from one of the first group of receive devices to the second memory during a second clock cycle, the second clock cycle immediately succeeding the first clock cycle, and

transfer data from one of the second group of receive devices to the first memory during the second clock cycle (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62, where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented).

Regarding claim 23, Humphrey teaches the system of claim 16, wherein the switching device is further configured to:

alternate the transfer of data frame information from the first group of receive devices to the first and second external memory buses each clock cycle, and

alternate the transfer of data frame information from the second group of receive devices to the first and second external memory buses each clock cycle (Column 3, lines 1 – 16; Column 5, lines 55 – 63; Column 7, lines 58 – 61; Column 8, lines 57 – 62,

where Humphrey discloses that the receive devices gain access too a first and second memory devices on a rotational or alternating system where the receive device first gains access to bank 0 at time slot 0, then is able to get access to bank 1 at time slot 1 or later. If there were only two receive devices, then the access to the first and second memory back would rotate from the first to the second to the first again on consecutive intervals, but Humphrey also discloses having more than just two receive devices where a more complex alternating method is implemented).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey in view of Mann, in further view of Runaldue (6052751) (Applicants IDS).

Regarding claim 7, Humphrey teaches the network device of claim 5.

Humphrey does not explicitly indicate that the first and second external memory buses are each 8-bytes wide and that the frequency is 100 MHz.

Mann discloses a memory interface with dual memories that discloses the transferred data can be 8 bytes wide (Column 1, lines 35 – 36; Column 2, lines 52 – 55 for the 8 bytes or 64 bits).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Humphrey's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Runaldo teaches that external memory can operate at 100 MHz (Column 5, line 32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Runaldo's teaching that external memory can operate at 100 MHz and enable Humphrey's switch to interface with memory at that speed.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 7, 9-13, 15-19, and 21-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Bates whose telephone number is (571) 272-3980. The examiner can normally be reached on 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on (571) 272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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